Amendments to the Claims

Claim 1 **(Currently Amended)** A receiver ~~adapted to detect~~ for detecting an approximate value of the power of a reception signal, the receiver comprising:

first operation means for adding a value obtained by multiplying a smaller one of a component I and a component Q of the reception signal by 1/8 and ~~the~~ a value of a larger one of ~~these~~ the components I and Q;

second operation means for adding a value obtained by multiplying the smaller one of the component I and the component Q of the reception signal by 1/2 and a value obtained by multiplying the larger one of ~~these~~ the components I and Q by 7/8; and

detection means for detecting ~~the~~ a value of a larger one of ~~the~~ an operation result of ~~the~~ said first operation means and ~~the~~ an operation result of ~~the~~ said second operation means as ~~an~~ the approximate value of the power of the reception signal.

Claim 2 **(Currently Amended)** A receiver ~~adapted to detect~~ for detecting an approximate value of the power of a reception signal, the receiver comprising:

a first comparator for comparing a component I and a component Q of ~~a~~ the reception signal with each other to determine which one of ~~these~~ the components I and Q is larger or smaller to thereby output a larger component as a first output value and output a smaller component as a second output value;

a 3-bit shift register for multiplying the first output value from ~~the~~ said first comparator by 1/8;

a subtractor for subtracting an output value from ~~the~~ said 3-bit shift register from the first output value from ~~the~~ said first comparator;

a 1-bit shift register for multiplying the second output value from ~~the~~ said first comparator by 1/2;

a 2-bit shift register for multiplying an output value from ~~the~~ said 1-bit shift register by 1/4;

a first adder for adding the first output value from ~~the~~ said first comparator and ~~the~~ an output value from ~~the~~ said 2-bit shift register;

a second adder for adding an output value from ~~the~~ said subtractor and ~~an~~ the output value from ~~the~~ said 1-bit shift register; and

a second comparator for comparing an output value from ~~the~~ said first adder and an output value from ~~the~~ said second adder with each other to determine which one of ~~these~~ the output values is larger or smaller and output ~~the~~ a value of a larger one thereof as ~~an~~ the approximate value of the power of the reception signal.

Claim 3 **(Currently Amended)** A mobile-station device ~~adapted to detect~~ for detecting an approximate value of the power of a signal radio-received from a base-station device, the mobile-station device including a receiver comprising:

first operation means for adding a value obtained by multiplying a smaller one of a component I and a component Q of the reception signal by 1/8 and ~~the~~ a value of a larger one of the components I and Q ~~thereof~~;

second operation means for adding a value obtained by multiplying ~~a~~ the smaller one of the component I and the component Q of the reception signal by 1/2 and a value obtained by multiplying ~~a~~ the larger one ~~thereof~~ of the components I and Q by 7/8; and

detection means for detecting a value of a larger one of ~~the~~ an operation result of ~~the~~ said first operation means and ~~the~~ an operation result of ~~the~~ said second operation means as ~~an~~ the approximate value of the power of the reception signal.

Claim 4 **(Currently Amended)** A mobile-station device ~~adapted to detect~~ for detecting an approximate value of the power of a signal radio-received from a base-station device, the mobile-station device including a receiver comprising:

a first comparator for comparing a component I and a component Q of ~~a~~ the reception

signal with each other to determine which one of ~~these~~ the components I and Q is larger or smaller to thereby output a larger component as a first output value and output a smaller component as a second output value;

a 3-bit shift register for multiplying the first output value from ~~the~~ said first comparator by 1/8;

_____a subtractor for subtracting an output value from ~~the~~ said 3-bit shift register from the first output value from ~~the~~ said first comparator;

_____a 1-bit shift register for multiplying the second output value from ~~the~~ said first comparator by 1/2;

_____a 2-bit shift register for multiplying an output value from ~~the~~ said 1-bit shift register by 1/4;

_____a first adder for adding the first output value from ~~the~~ said first comparator and ~~the~~ an output value from ~~the~~ said 2-bit shift register;

_____a second adder for adding an output value from ~~the~~ said subtractor and ~~an~~ the output value from ~~the~~ said 1-bit shift register; and

_____a second comparator for comparing an output value from ~~the~~ said first adder and an output value from ~~the~~ said second adder with each other to determine which one of ~~these~~ the output values is larger or smaller and output ~~the~~ a value of a larger one thereof as ~~an~~ the approximate value of the power of the reception signal.

Claim 5 **(Currently Amended)** A detection method ~~adapted to detect~~ for detecting an approximate value of the power of a signal received from a receiver, the detection method comprising ~~the steps of~~:

adding a value obtained by multiplying a smaller one of a component I and a component Q of the reception signal by 1/8 and a value of a larger one of the components I and Q ~~thereof~~ to set ~~the~~ an addition result ~~to be~~ as a first operation result;~~,~~

_____adding a value obtained by multiplying the smaller one of the component I and the component Q of the reception signal by 1/2 and a value obtained by multiplying the larger one ~~thereof~~ of the components I and Q by 7/8 to set ~~the~~ an addition result ~~to be~~ as a second operation result;~~,~~ and

_____detecting a value of a larger one of the first operation result and the second operation result as ~~an~~ the approximate value of the power of the reception signal.

Claim 6 **(Currently Amended)** A detection method ~~adapted to detect~~ for detecting an approximate value of the power of a signal received from a receiver, the detection method comprising ~~the steps of~~:

comparing a component I and a component Q of the reception signal with each other to determine which one of ~~these~~ the components I and Q is larger or smaller through ~~the~~ operation of a first comparator, to thereby output a larger component as a first output value and output a smaller component as a second output value;

_____multiplying the first output value from the first comparator by 1/8 through ~~the~~ operation of a 3-bit shift register;

_____subtracting an output value from the 3-bit shift register from the first output value from the first comparator through ~~the~~ operation of a subtractor;

_____multiplying the second output value from the first comparator by 1/2 through ~~the~~ operation of a 1-bit shift register;

_____multiplying an output value from the 1-bit shift register by 1/4 through ~~the~~ operation of a 2-bit shift register;

_____adding the first output value from the first comparator and ~~the~~ an output value from the 2-bit shift register through ~~the~~ operation of a first adder;

_____adding an output value from the subtractor and ~~an~~ the output value from the 1-bit shift register through ~~the~~ operation of a second adder; and

_____comparing an output value from the first adder and an output value from the second adder with each other through ~~the~~ operation of a second comparator, to thereby determine which one of ~~these~~ the output values is larger or smaller and detect ~~the~~ a value of a larger one thereof as ~~an~~ the approximate value of the power of the reception signal.

Claim 7 **(Currently Amended)** A receiver ~~adapted to detect~~ for detecting and outputting an approximate value of the power of a reception signal, the receiver operable to ~~wherein~~:

~~operations are performed~~perform a plurality of operations using a plurality of approximate equations that are different from each other to calculate from the same reception signal, a plurality of candidates ~~each becoming an~~ for the approximate value of the power of the reception signal ~~are calculated,~~; and

_____~~an excellent one is detected~~ detect an excellent candidate from among ~~a~~ the plurality of ~~the~~ candidates as ~~an~~ the approximate value of the power of the reception signal to be outputted.

Claim 8 **(Currently Amended)** A mobile-station device ~~adapted to detect~~ for detecting and outputting an approximate value of the power of a signal radio-received from a base-station device, the mobile-station device comprising a receiver ~~that performs~~ operable to:

perform a plurality of operations using a plurality of approximate equations, ~~calculates~~ that are different from each other to calculate from the same reception signal a plurality of candidates ~~each becoming an~~ for the approximate value of the power of the reception signal,; and

~~detects~~detect an excellent ~~one~~ candidate from among ~~a~~ the plurality of ~~the~~ candidates as ~~an~~ the approximate value of the power of the reception signal to be outputted.

Claim 9 **(Currently Amended)** A detection method ~~adapted to detect~~ for detecting and outputting an approximate value of the power of a signal received from a receiver, the detection method comprising ~~the steps of~~:

performing a plurality of operations using a plurality of approximate equations, ~~calculating~~ that are different from each other and each include at least one bit shift operation, at least one add or subtract operation and at least one compare operation, to calculate from the same reception signal a plurality of candidates ~~each becoming an~~ for the approximate value of the power of the reception signal,; and

detecting an excellent ~~one~~ candidate from among ~~a~~ the plurality of ~~the~~ candidates as ~~an~~ the approximate value of the power of the reception signal to outputted.